

SM74611 Smart Bypass Diode

1 Features

- Maximum Reverse Voltage (V_R) of 30 V
- Operating Forward Current (I_F) of up to 15 A
- Low Average Forward Voltage (26 mV at 8 A)
- Less Power Dissipation than Schottky Diode
- Lower Leakage Current than Schottky Diode
- Footprint and Pin-Compatible With Conventional D2PAK Schottky Diode
- Operating Range (T_J) of -40°C to 125°C

2 Applications

- Bypass Diodes for Photovoltaic Panels
- Bypass Diodes for Microinverter and Power Optimizer

3 Description

The SM74611 device is a smart bypass diode used in photovoltaic applications. The SM74611 device serves the purpose of providing an alternate path for string current when parts of the panel are shaded during normal operation. Without bypass diodes, the shaded cells will exhibit a hot spot which is caused by excessive power dissipation in the reverse biased cells.

Currently, conventional P-N junction diodes or Schottky diodes are used to mitigate this issue. Unfortunately the forward voltage drop for these diodes is still considered high (approximately 0.6 V for normal diodes and 0.4 V for Schottky). With 10 A of currents flowing through these diodes, the power dissipation can reach as high as 6 W. This in turn will raise the temperature inside the junction box where these diodes normally reside and reduce module reliability.

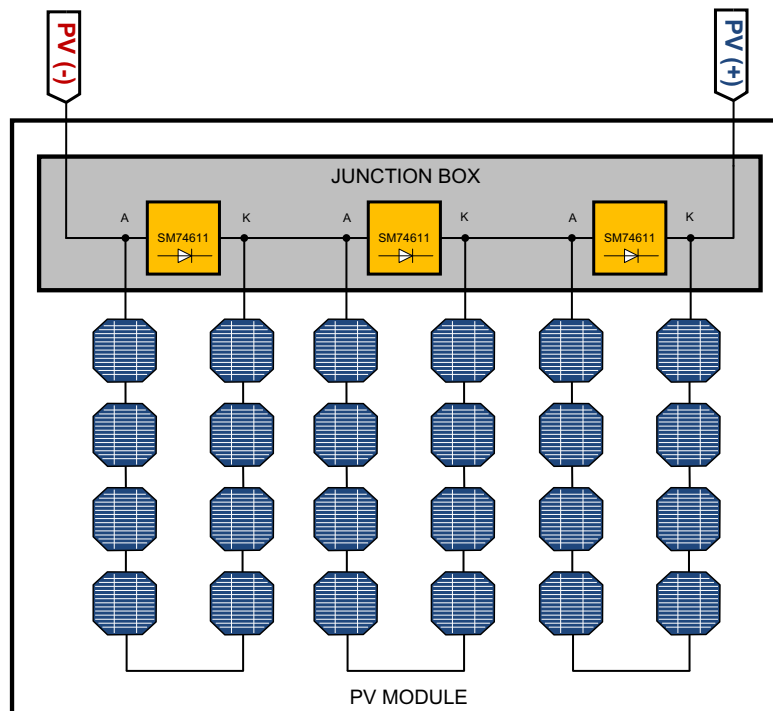
The advantage of the SM74611 is that it has a lower forward voltage drop than P-N junction and Schottky diodes. It has a typical average forward voltage drop of 26 mV at 8 A of current. This translates into typical power dissipation of 208 mW, which is significantly lower than the 3.2 W of conventional Schottky diodes. The SM74611 is also footprint and pin compatible with conventional D2PAK Schottky diodes, making it a drop-in replacement in many applications.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SM74611	TO-263 (3)	10.18 mm x 8.41 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application in a Junction Box



Copyright © 2016, Texas Instruments Incorporated



Table of Contents

1 Features	1	7.3 Feature Description.....	6
2 Applications	1	7.4 Device Functional Modes.....	7
3 Description	1	8 Application and Implementation	8
4 Revision History	2	8.1 Application Information.....	8
5 Pin Configuration and Functions	3	8.2 Typical Application	8
6 Specifications	3	9 Power Supply Recommendations	11
6.1 Absolute Maximum Ratings	3	10 Layout	11
6.2 ESD Ratings.....	4	10.1 Layout Guidelines	11
6.3 Recommended Operating Conditions.....	4	10.2 Layout Example	11
6.4 Thermal Information	4	11 Device and Documentation Support	12
6.5 Electrical Characteristics.....	4	11.1 Community Resources.....	12
6.6 Typical Characteristics	5	11.2 Trademarks	12
7 Detailed Description	6	11.3 Electrostatic Discharge Caution.....	12
7.1 Overview	6	11.4 Glossary	12
7.2 Functional Block Diagram	6	12 Mechanical, Packaging, and Orderable Information	12

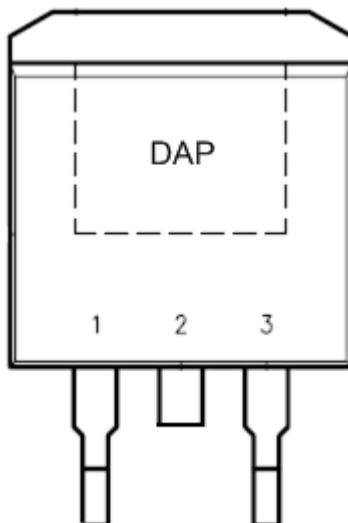
4 Revision History

Changes from Revision A (November 2014) to Revision B	Page
<ul style="list-style-type: none"> Added <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section 	1

Changes from Original (December 2012) to Revision A	Page
<ul style="list-style-type: none"> Added new junction temperature for $t \leq 1$ hour 	3
<ul style="list-style-type: none"> Added Thermal Table 	4
<ul style="list-style-type: none"> Changed typical characteristic curves 	5

5 Pin Configuration and Functions

**KTT Package
3-Pin TO-263
Top View**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ANODE	1 ⁽¹⁾	I	Connect both of these pins to the negative side of the PV cells
	3 ⁽¹⁾		
CATHODE	2 ⁽²⁾	O	Pin 2 and the DAP are shorted internally. Connect the DAP to the positive side of the PV cells
	DAP ⁽²⁾		

- (1) Pin 1 and Pin 3 must be connected together for proper operation.
(2) Package drawing at the end of datasheet is shown without Pin 2 being trimmed.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

	MIN	MAX	UNIT
DC reverse voltage		30	V
Forward current		24	A
Junction temperature, $t \leq 1$ hour		135	°C
Storage temperature, T_{stg}	-65	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) System must be thermally managed so as not to exceed maximum junction temperature

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
DC reverse voltage		28	V
Junction temperature (T_J)	−40	125	°C
Forward current	0	15	A

- (1) System must be thermally managed so as not to exceed maximum junction temperature

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SM74611	UNIT
		KTT (TO-263)	
		3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	22.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{F(AVG)}$	Forward current				8	15	A
$V_{F(AVG)}$	Forward voltage	$I_F = 8$ A	$T_J = 25^\circ\text{C}$		26		mV
P_D	Power dissipation	$I_F = 8$ A	$T_J = 25^\circ\text{C}$		208		mW
			$T_J = 125^\circ\text{C}$		450		
			−40°C to 125°C ⁽¹⁾			575	
		$I_F = 15$ A	$T_J = 25^\circ\text{C}$		695		
			$T_J = 125^\circ\text{C}$		1389		
D	Duty cycle	$I_F = 8$ A	$T_J = 25^\circ\text{C}$		99.5%		
			$T_J = 125^\circ\text{C}$		96.0%		
I_R	Reverse leakage current	$V_{REVERSE} = 28$ V	$T_J = 25^\circ\text{C}$		0.3		μA
			$T_J = 125^\circ\text{C}$		3.3		

- (1) Limits −40°C to 125°C apply over the entire junction temperature range for operation. Limits appearing in normal type apply for $T_A = T_J = 25^\circ\text{C}$.

6.6 Typical Characteristics

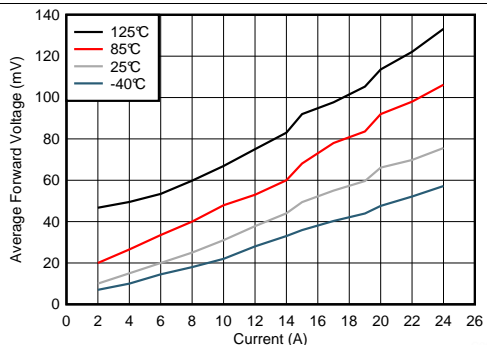


Figure 1. Average Forward Voltage (Anode to Cathode) Over Temperature

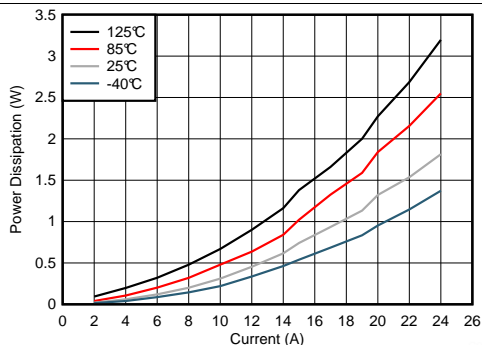


Figure 2. Power Dissipation Over Temperature

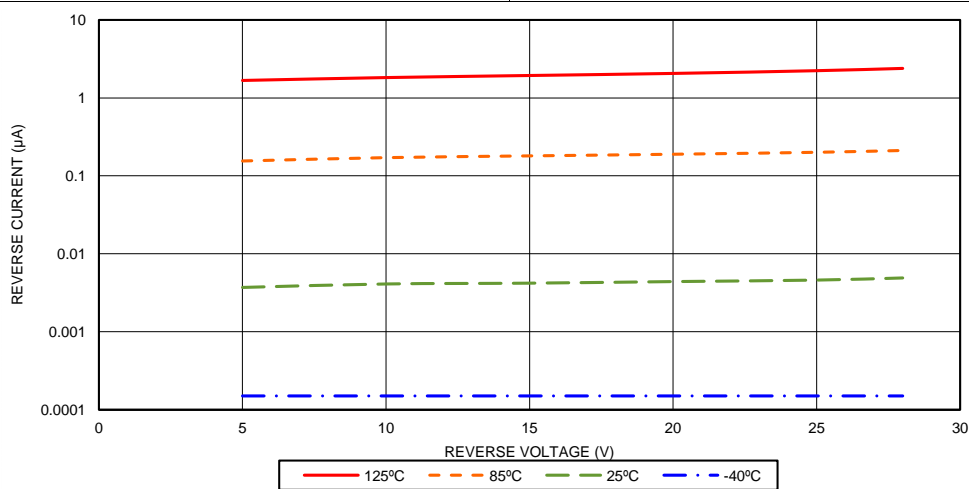


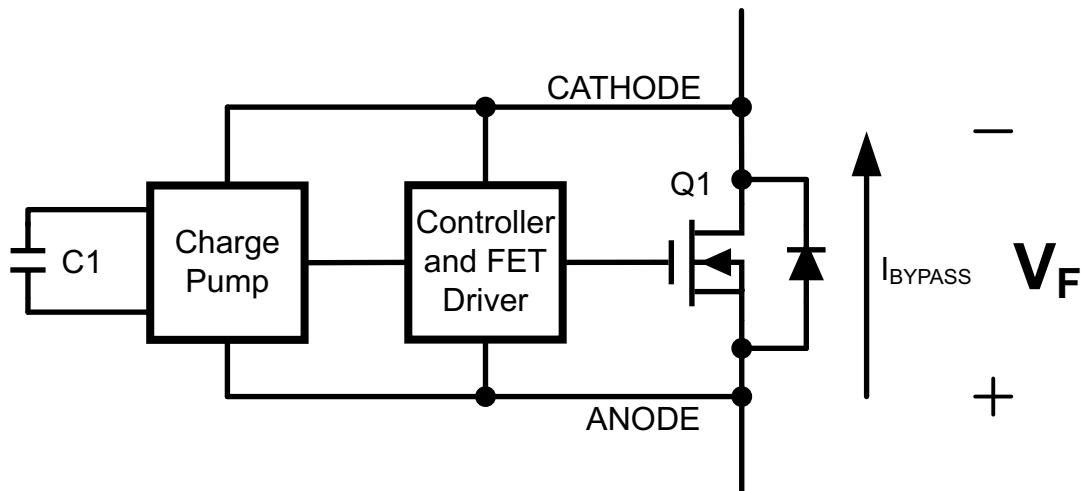
Figure 3. Reverse Current Over Temperature (Cathode to Anode)

7 Detailed Description

7.1 Overview

The SM74611 is designed for use as a bypass diode in photovoltaic modules. The SM74611 uses a charge pump to drive an N-channel FET to provide a resistive path for the bypass current to flow.

7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

Figure 4. SM74611 Block Diagram

7.3 Feature Description

The operational description is described in the following sections. See [Figure 4](#) and [Figure 5](#).

7.3.1 From t_0 to t_1

When cells in the solar panels are shaded, the FET Q1 is off and the bypass current flows through the body diode of the FET as shown on [Figure 4](#). This current produces a voltage drop (V_F) across ANODE and CATHODE terminal of the bypass diode. During this time, the charge pump circuitry is active and charging capacitor C1 to a higher voltage.

7.3.2 At t_1

Once the voltage on the capacitor reaches its predetermined voltage level, the charge pump is disabled and the capacitor voltage is used to drive the FET through the FET driver stage.

7.3.3 From t_1 to t_2

When the FET is active, it provides a low resistive path for the bypass current to flow thus minimizing the power dissipation across ANODE and CATHODE. Because the FET is active, the voltage across the ANODE and CATHODE is too low to operate the charge pump. During this time, the stored charge on C1 is used to supply the controller as well as drive the FET.

7.3.4 At t_2

When the voltage on the capacitor C1 reaches its predetermined lower level, the FET driver shuts off the FET. The bypass current will then begin to flow through the body diode of the FET, causing the FET body diode voltage drop of approximately 0.6 V to appear across ANODE and CATHODE. The charge pump circuitry is re-activated and begins charging the capacitor C1. This cycle repeats until the shade on the panel is removed and the string current begins to flow through the PV cells instead of the body diode of the FET.

Feature Description (continued)

The key factor to minimizing the power dissipation on the device is to keep the FET on at a high duty cycle. The average forward voltage drop will then be reduced to a much lower voltage than for a Schottky or regular P-N junction diode.

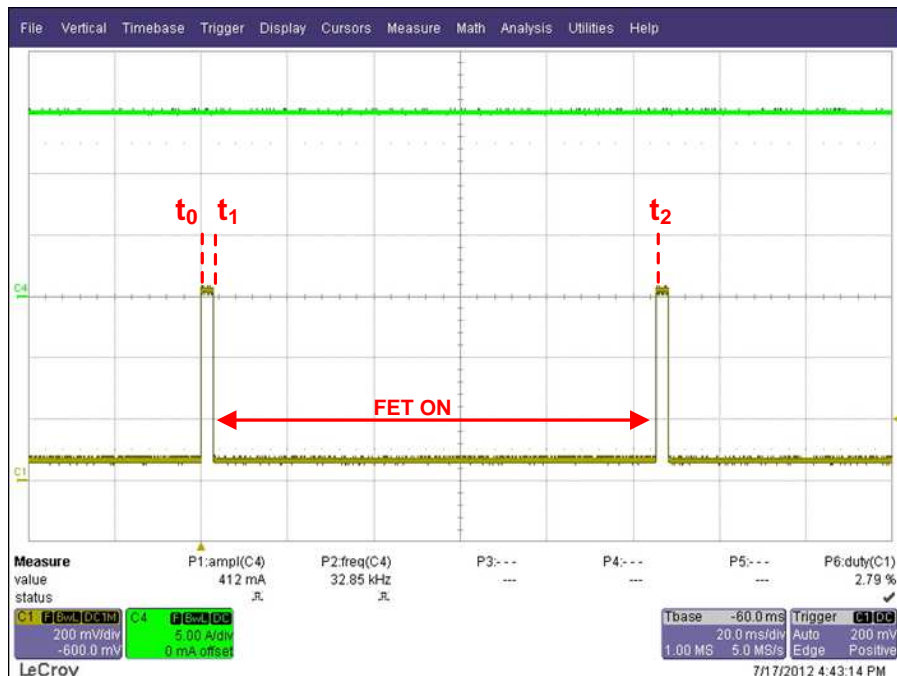


Figure 5. ANODE to CATHODE Voltage (Ch1) With $I_{\text{BYPASS}} = 15 \text{ A}$ (Ch4) for SM74611 in Junction Box at 85°C Ambient

7.4 Device Functional Modes

7.4.1 FET Q1 OFF

Initially, the internal FET Q1 is OFF. This is between t_0 and t_1 as shown in Figure 5. When current begins flowing from ANODE to CATHODE, the FET Q1 body diode conducts with a voltage drop V_F .

7.4.2 FET Q1 ON

The FET Q1 is ON between t_1 and t_2 as shown in Figure 5. During this time, the FET gate is driven and current flows through the FET through a low resistive path.

8 Application and Implementation

NOTE

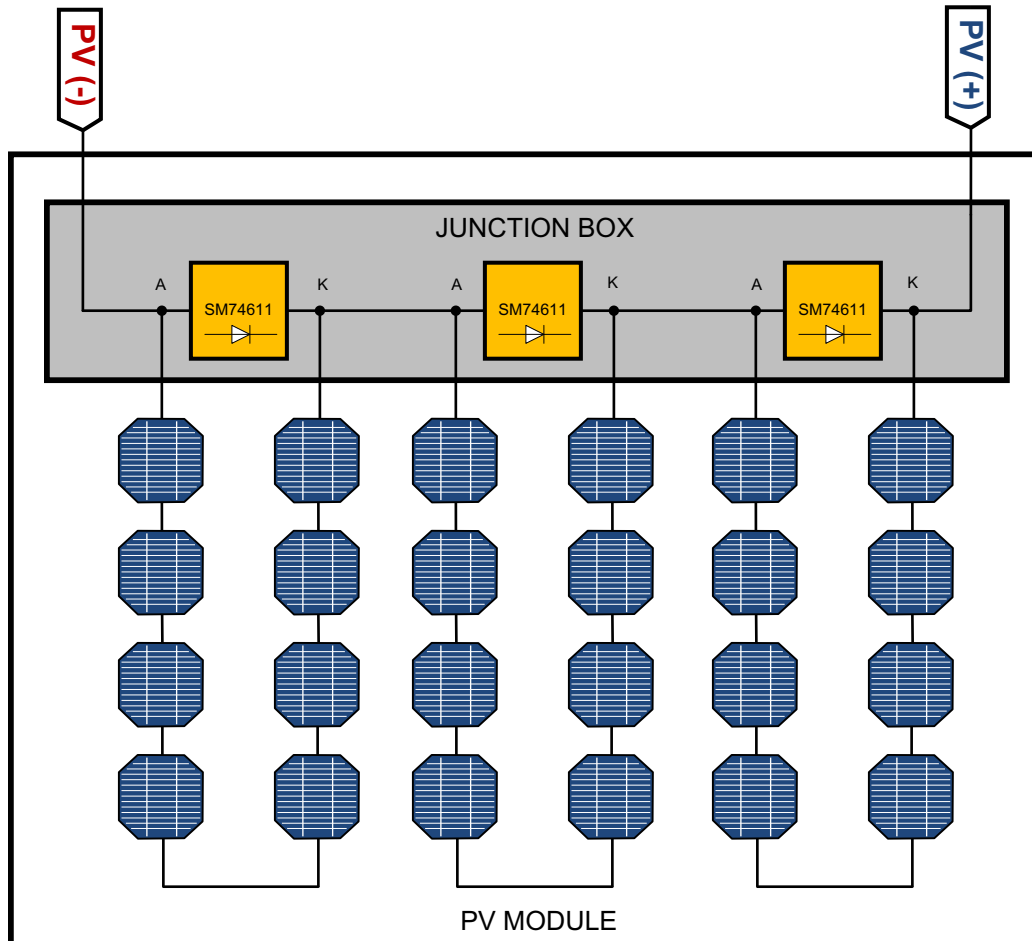
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SM74611 smart bypass diode is a drop-in replacement for traditional bypass diodes used in photovoltaic (PV) applications. When compared to a typical diode, which has a typical 0.7-V drop during forward conduction, the SM74611 dissipates significantly less power and allows PV applications such as solar junction boxes to run much cooler.

8.2 Typical Application

The application diagram shown in [Figure 6](#) shows 3 SM74611 Smart Bypass Diodes connected in series, each providing a bypass path for 8 solar cells for a total of 24 solar cells.



Copyright © 2016, Texas Instruments Incorporated

Figure 6. Solar Junction Box

Typical Application (continued)

8.2.1 Design Requirements

Table 1 lists the parameters for Figure 6

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Minimum input voltage $V_{IN_{MIN}}$	1 V
Maximum input voltage $V_{IN_{MAX}}$	28 V
Maximum forward current I_{MAX}	20 A
Junction temperature range T_J	–40°C to 125°C

8.2.2 Detailed Design Procedure

The SM74611 is primarily used in solar junction boxes to improve the efficiency compared to commonly used P-N junction or Schottky diodes. The junction boxes have 2 or 3 diodes in series connected across the solar panel, each diode connected across a substring of solar cells, as shown in Figure 6. Standard bodies like IEC and UL mandate certain thermal tests for bypass diodes in junction boxes. At the time of this writing, the applicable specifications include IEC61215, IEC61646, EN 50548, IEC62790, and UL3730. The test procedures across these specifications are similar and include the following:

- Apply temperature probe to the diode (in the case of SM74611 the smart bypass diode) body
- Apply $75 \pm 50^\circ\text{C}$ to the junction box, containing the 2 to 3 (smart bypass) diodes
- Apply panel-rated, short-circuit current through the box for 1 hour
- Increase the current to 1.25 times the rated value and continue testing for another 1 hour

While the specifications may not specify how the temperature must be maintained, it is expected that there will be no air flow as in a real application behind a solar panel. Also there may be no specification of how the temperature is raised from room to 750°C . TI recommends a gradual and controlled increase to avoid shock to the product under test. Using a good climate chamber or oven is needed to ensure uniformity and consistency of temperature during test and from test of one junction box to another. Similar precautions are also necessary with the thermocouples and temperature probes used during the tests. It is a good idea to check the equipment used with the certification body. The junction box should be operational after these tests. Due to body diode pulses, a simple diode tester cannot be used to test the Smart Bypass Diode. An example testing scheme is shown in [Application Curve](#). To avoid component failure, the Smart Bypass Diode junction temperature must not exceed the maximum rating during these tests. See [Absolute Maximum Ratings](#) for the SM74611 limits. The junction temperature is calculated based on the measured values from the temperature probe.

The temperature probe could be applied on the top (plastic case) or bottom (tab) of the SM74611 body, as shown in Figure 7. Methods of applying this probe vary from Kapton tape, 2K-resins (for top) to soldering (bottom tab). It is good to check with the certification body regarding the acceptable method.

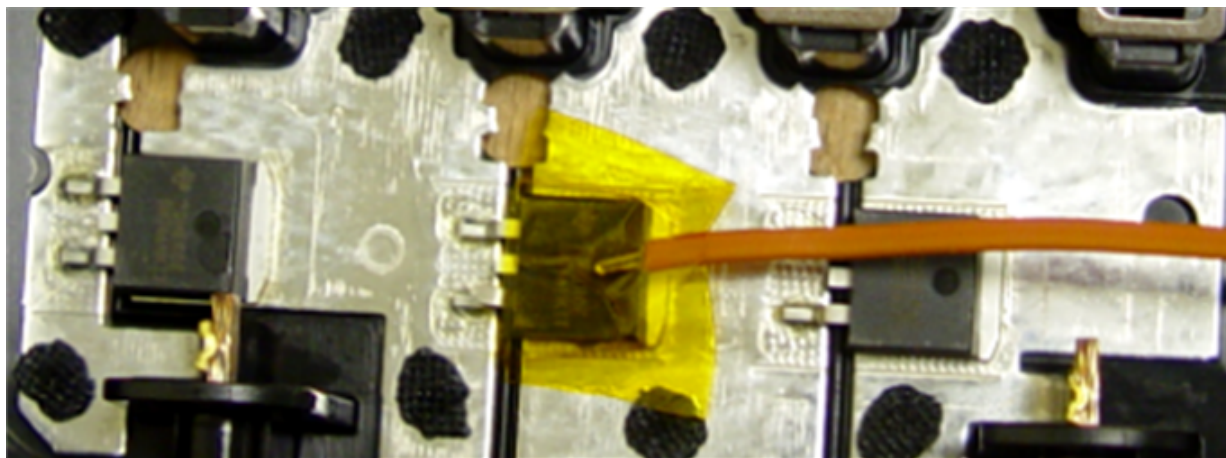


Figure 7. Temperature Probe Attachment During Thermal Test

Because the SM74611 Smart Bypass Diode cycles the FET ON and OFF to recharge the charge pump, occasionally the body diode conducts instead of the FET. Therefore the drop across the Smart Bypass Diode is not constant even at constant load. Due to this switching behavior, a normal diode tester can not be used to test the operation of the Smart Bypass Diode. The following test scheme is provided, as an example, with junction box application consideration. See [Figure 8](#) while reading the following test steps:

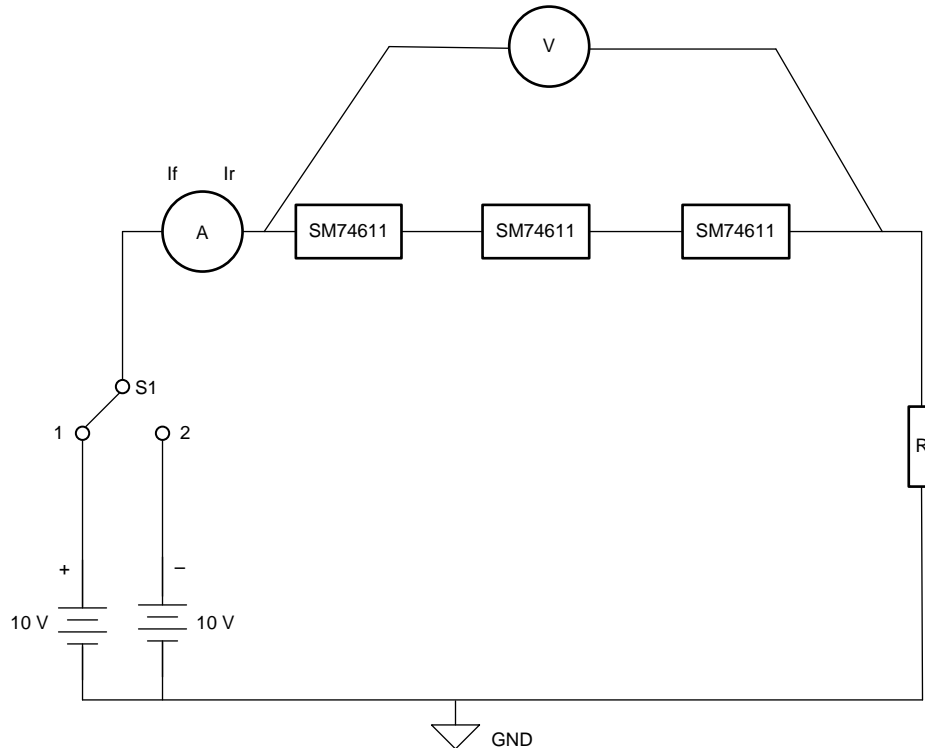


Figure 8. Example Test Setup for SM74611

Step 1: Testing Forward voltage drop (set R such that $I_f \Rightarrow 1\text{ A}$)

- Toggle S1 to position 1
- Make sure to see I_f reading of $10\text{V}/R$
- Measure Voltage across 3 SM74611 or 1 ea SM74611
- If the setup is working properly, V_f will be less than 150 mV (R_{dson} losses)

Potential Fault Conditions

- SM74611 FET is not turning ON -> the measured voltage will be $> 500\text{ mV}$
- SM74611 device is not soldered and open -> No I_f current is seen

Step 2: Testing Reverse voltage turn OFF

- Toggle S1 to position 2
- Measure current I_r which is expected to be $< 1\ \mu\text{A}$

Potential Fault Conditions

- SM74611 FET is shorted or board short is present, the measured current I_r is same as I_f but with reverse polarity. (This is only in the case of testing each SM74611 and not applicable for testing 3 together).

8.2.3 Application Curve

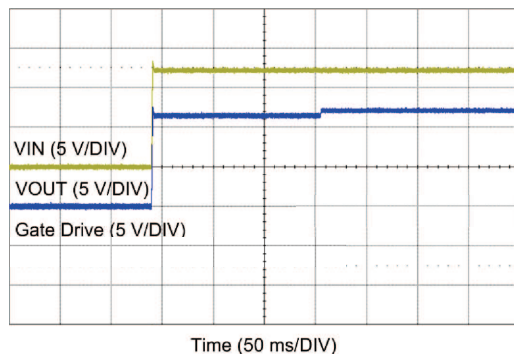


Figure 9. Start-Up Related to Input Voltage from the Panel

9 Power Supply Recommendations

The SM74611 is designed to be implemented as bypass diode in photovoltaic modules. System designer must ensure that the voltage level from solar modules does not exceed 28 V. At the time of this writing, the applicable specifications include IEC61215, IEC61646, EN 50548, IEC62790, and UL3730. This is because the SM74611 can protect against a maximum of -28 V as a bypass diode. The internal MOSFET of SM74611 can pass up to 15-A current. Drawing more current can damage the internal MOSFET permanently.

10 Layout

10.1 Layout Guidelines

Some layout guidelines must be followed to ensure proper conduction from ANODE to CATHODE pins. ANODE and CATHODE traces carrying the load current must be wide to reduce the amount of parasitic trace inductance as shown in Figure 10.

10.2 Layout Example

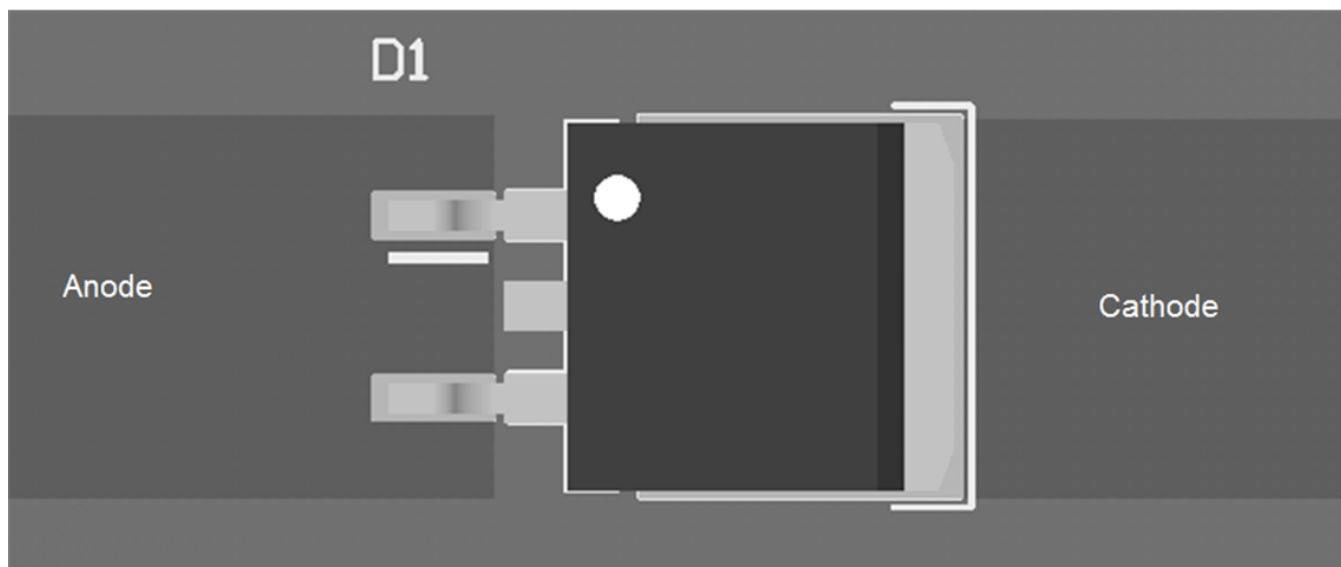


Figure 10. Layout Example for SM74611

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SM74611KTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	SM74611KTT	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SM74611KTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

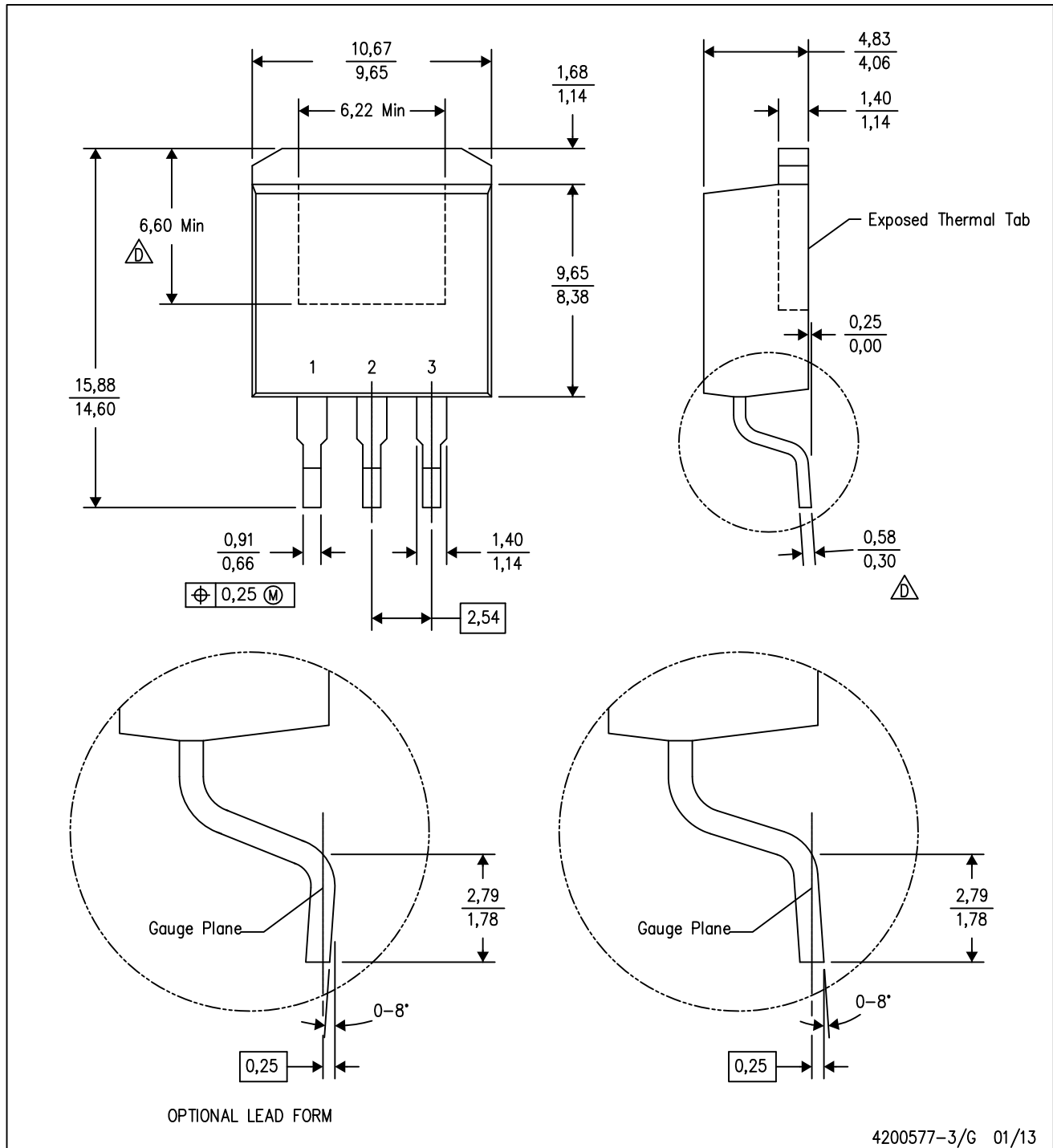


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SM74611KTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0

KTT (R-PSFM-G3)

PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- Falls within JEDEC TO-263 variation AA, except minimum lead thickness and minimum exposed pad length.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com